REMARKS

Claims 1-28 are pending. By this Amendment, the drawings are corrected pursuant to the attached drawing sheet, claims 5 and 24 are cancelled without prejudice to or disclaimer of the subject matter contained therein, and claims 1, 4, 6, 19, 20, 23 and 25 are amended. Claims 1, 19 and 20 are amended to recite features supported in the specification on page 9, line 14 – page 10, line 19. Claims 1 and 20 are also amended to recite features from claims 5 and 24, respectively. Claims 6 and 25 are amended to revise claim dependencies. No new matter is added by any of these amendments.

Applicants appreciate the courtesies extended to Applicants' representative by Examiners Ferris and Jones during the March 26, 2003 interview. In accordance with MPEP §713.04, the points discussed during the interview are incorporated in the remarks below and constitute Applicants' record of the interview.

Reconsideration based on the following remarks is respectfully requested.

I. Amendment Entry after Final Rejection

Entry of this amendment is proper under 37 CFR §1.116 because the amendments: a) place the application in condition for allowance (for all the reasons discussed herein); b) do not raise any new issues requiring further search or consideration; c) place the application in better condition for appeal (if necessary); and d) address formal requirements of the Final Rejection and preceding Office Action.

The foregoing amendments do not raise any new issues after Final Rejection. Therefore, entry of the amendments is proper under 37 CFR §1.116 because the amendments place the application in condition for allowance. Accordingly, Applicants respectfully request entry of this Amendment.

II. Disclosed Reference Is No Longer Applicable

The March 21, 2000 Information Disclosure Statement submitted a reference to Application 09/194,445 that was abandoned on May 2, 2002. Thus, this reference need no longer be considered.

III. Claimed Subject Matter is Supported in the Specification

The Final Office Action asserts on pp. 2-3 that the subject matter of the claims is inconsistent with the specification at page 2, lines 3-10 and page 11, lines 11-27. Applicants assert that the subject matter of the claims is supported in the specification at, *inter alia*, page 8, line 20 – page 9, line 13, page 10, lines 2-26 and page 12, lines 10-18.

IV. Claims 1-28 Define Patentable Subject Matter

The Final Office Action rejects claims 1, 19 and 20 under 35 U.S.C. §102(b) over U.S. Patent 6,240,377 to Kai *et al.* (Kai). This rejection is respectfully traversed.

Kai does not teach or suggest a microcomputer for performing information processing, including a processor for executing instructions, external terminals for an external bus being connectable to both an emulation memory and an external memory other than the emulation memory, the external terminals being connected to at least the emulation memory through the external bus when the microcomputer is in an emulation mode and being connected to the external memory without being connected to the emulation memory when the microcomputer is not in the emulation mode, and bus control means for connecting a bus of the processor to the external bus so that an access of the processor to an internal memory will be switched to an access to the emulation memory through the external bus when the microcomputer is in the emulation mode, wherein the microcomputer further comprises memory control means for outputting a first control signal for controlling the external memory connected to the external bus and a second control signal for controlling the emulation memory connected to the external bus, the second control signal being different from the first control signal, as recited in claim 1, and similarly recited in claim 20.

Kai further fails to teach or suggest an emulation method for a microcomputer including a processor for executing instructions, and external signals for an external bus being connectable to an emulation memory and an external memory other than the emulation memory, the external terminals being connected to at least the emulation memory through the external bus when the microcomputer is in an emulation mode and being connected to the external memory without being connected to the emulation memory when the microcomputer is not in the emulation mode, wherein the external bus is shared between the emulation memory and the external memory, and the emulation memory is accessed through the external bus when the microcomputer is on evaluation, thereby causing the processor to operate according to information read out from the emulation memory, and wherein the processor is operated according to information read out from the internal memory when the microcomputer is on production, as recited in claim 19.

Instead, Kai discloses an EEPROM for emulation. In particular, Kai teaches an in-circuit emulator 30 and an emulation chip 31. The emulator 30 includes an emulation memory 37 and an emulation circuit 38. The emulation chip 31 includes a CPU 33, an EEPROM 34 and an accessibility controller 40. From the CPU 33, interconnect busses 32, 36 and 39 provide connections to the emulation memory 37, a peripheral circuit 35 and the EEPROM controller 40. An interconnect bus 45 connects between the EEPROM controller and the EEPROM. The EEPROM controller 40 accesses the EEPROM 34 via the peripheral circuit interconnect bus 36 during emulation or the memory interconnect bus 39 during normal operation. See col. 3, line 46 – col. 4, line 37, col. 4, lines 62-66 and Fig. 1 of Kai.

Nowhere does Kai disclose an external terminal which is connected to at least an emulation memory when the emulation mode is turned ON, and connected to an external memory when the emulation mode is turned OFF. For example, the bus 32 in Fig. 1 of Kai is labeled an emulator interconnect bus. This means that the bus 32 of Kai is used only for emulation. That is, the bus 32 of Kai corresponds to a busses 712 and 714 in Fig. 1B of the

present application. Providing a bus 32 of Kai used only for emulation would produce the problems described in the present specification described at page 1, line 14 to page 2, line 12.

In contrast, Applicants' claimed features provide an external terminal, which is connected to at least an emulation memory when the emulation mode becomes ON, and connected, not to an emulation memory, but to an external memory when the emulation mode becomes OFF. In other words, the external terminal of the microcomputer computer (*i.e.*, the external bus) is shared between the emulation memory and the external memory. Therefore, the optimum circumstances of evaluation can be realized, while saving the number of terminals in the microcomputer, by way of example. For more details, please see the present specification at page 10, line 27 to page 12, line 9.

Further, Kai fails to teach or suggest the features incorporating the subject matter of claims 5 and 24 and recited in claims 1 and 20. For example, in Fig. 2 of the present application, a memory controller outputs a first control signal CNT1 for the external memory and a second control signal CNT2 for the emulation memory. This enables sharing the external bus (*i.e.*, external terminal) between the external memory and the emulation memory. Kai fails to disclose this configuration.

A claim must be anticipated for a proper rejection under §102(a), (b) and (e). This requirement is satisfied "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." See MPEP §2131. Kai lacks an external memory other than the emulation memory and a memory control means for connecting a first access between an internal memory and to either the emulation memory or else the external memory, as recited in the claims. Thus, Kai fails to anticipate Applicants' claimed subject matter. Withdrawal of the §102 rejection is respectfully requested.

The Final Office Action further rejects claim1, 19 and 20 under 35 U.S.C. §103(a) over U.S. Patent 5,313,618 to Pawlowski (Pawlowski '618) in view of U.S. Patent 5,623,673 to Gephardt *et al.* (Gephardt). The Final Office Action further rejects claims 2-18 and 21-28

under 35 U.S.C. §103(a) over U.S. Patent 4,939,637 to Pawlowski (Pawlowski '637) in view of Gephardt. These rejections are respectfully traversed.

Neither Pawlowski '618 nor Gephardt, alone or in combination, teaches or suggests a microcomputer for performing information processing, including a processor for executing instructions, external terminals for an external bus being connectable to both an emulation memory and an external memory other than the emulation memory, the external terminals being connected to at least the emulation memory through the external bus when the microcomputer is in an emulation mode and being connected to the external memory without being connected to the emulation memory when the microcomputer is not in the emulation mode, and bus control means for connecting a bus of the processor to the external bus so that an access of the processor to an internal memory will be switched to an access to the emulation memory through the external bus when the microcomputer is in the emulation mode, wherein the microcomputer further comprises memory control means for outputting a first control signal for controlling the external memory connected to the external bus and a second control signal for controlling the emulation memory connected to the external bus, the second control signal being different from the first control signal, as recited in claim 1, and similarly recited in claim 20.

Nor do either Pawlowski '618 or Gephardt, alone or in combination, teach or suggest an emulation method for a microcomputer including a processor for executing instructions, and external signals for an external bus being connectable to an emulation memory and an external memory other than the emulation memory, the external terminals being connected to at least the emulation memory through the external bus when the microcomputer is in an emulation mode and being connected to the external memory without being connected to the emulation memory when the microcomputer is not in the emulation mode, wherein the external bus is shared between the emulation memory and the external memory, and the emulation memory is accessed through the external bus when the microcomputer is on

evaluation, thereby causing the processor to operate according to information read out from the emulation memory, and the processor is operated according to information read out from the internal memory when the microcomputer is on production, as recited in claim 19.

Instead, Pawlowski '618 discloses an emulator system with shared emulator memory. In particular, Pawlowski '618 teaches an emulation memory 206 connected to a controller 202 and an emulation microcontroller 204. The emulation memory 206 is connected to the controllers 202, 204 via address and data busses 208, 210, and is accessed via an address latch 212 and a multiplexer 220. The controller 202 also accesses firmware memory 262 via an address latch 260. See col. 9, lines 13-30, col. 9, line 64 – col. 10, line 6, col. 10, lines 25-42, col. 10, lines 62-67 and Fig. 2 of Pawlowski '618.

Nowhere does Pawloski '618 disclose an external terminal which is connected to at least an emulation memory when the emulation mode is turned ON, and connected to an external memory when the emulation mode is turned OFF. Instead, the busses 208 and 210 of Pawloski '618 correspond to a busses 712 and 714 in Fig. 1B of the present application. Also, by providing two processors, both accessing a single emulation memory instead of a processor accessing separate external and emulation memories, Pawlowski '618 teaches away from Applicants' claimed features.

In contrast, Applicants' claimed features provide an external terminal, which is connected to at least an emulation memory when the emulation mode becomes ON, and connected, not to an emulation memory, but to an external memory when the emulation mode becomes OFF. In other words, the external terminal of the microcomputer computer (*i.e.*, the external bus) is shared between the emulation memory and the external memory. Therefore, the optimum circumstances of evaluation can be realized, while saving the number of terminals in the microcomputer, by way of example. For more details, please see the present specification at page 10, line 27 to page 12, line 9.

Gephardt does not compensate for the deficiencies of Pawlowski '618 outlined above for claims 1, 19 and 20. Instead, Gephardt discloses an emulation memory mapping and locking method. In particular, Gephardt teaches a computer system 200 having a processor core 202 coupled to an interrupt control unit 204 and a memory control 208 that connects to a system memory 210. The memory control unit 208 includes a data buffer 212, address control 214 and a lock-out register 216. When the processor core 202 accesses normal memory space, the memory control unit 208 translates to system memory addresses. The interrupt control unit 204 transitions the state of the processor core 202 to "debug" mode, and reads the value of an ICE vector. See col. 4, lines 25-33, col. 5, lines 61-66, col. 8, lines 31-41 and Fig. 2 of Gephardt. Thus, Gephardt fails to teach or suggest either an emulation memory or an external memory, as recited in Applicants' claims.

Pawlowski '637 also does not compensate for the deficiencies of Gephardt outlined above for claims 1, 19 and 20. Nor does Pawlowski '637 teach, disclose or suggest the additional features recited in claims 2-18 and 21-28. Instead, Pawlowski '637 discloses a circuitry for an emulation mode. In particular, Pawlowski '637 teaches a processor 100 connected to data bus lines 101 and address bus lines 102, with emulation mode input from a block 124 to AND gates 129 and 130 via conductor 128. The block 124 includes a D-type latch 142 to produce a circuit for generating an "emulator mode" signal at the Q output. See col. 9, line 19 – col. 10, line 45 and Figs. 5 and 6 of Pawlowski '637.

Further, there is no motivation to combine features related to a dual-processor emulator of Pawlowski '618 with a mapping and lock-out method of Gephardt or emulator mode signal generating circuit of Pawlowski '637 with the memory mapping and lock-out method of Gephardt, nor has the Office Action established sufficient motivation or a *prima facie* case of obviousness.

Applicants further assert that the Examiner's allegation that it would have been obvious to one of ordinary skill in the art to implement "microprocessors including an

external bus connected to an external memory having different control signals" (page 4 of the Final Office Action) is merely a conclusory statement, and that no support for such a statement has been provided. When relying on what is asserted to be common knowledge to negate patentability, that knowledge must be articulated and placed on the record. Providing only conclusory statements when dealing with particular combinations of prior art in specific claims cannot support an assertion of obviousness. *In re Lee*, 61 USPQ 2d 1430, 1434-35 (Fed. Cir. 2002).

Although the Examiner may take official notice of facts outside of the record which are capable of instant and unquestionable demonstration as being "well known" in the art, "if the applicant traverses such an assertion, the Examiner should cite a reference in support of his or her position." See MPEP §2144.03. Thus, Applicants submit that the reliance on unsupported *per se* knowledge does not negate the patentability of the subject matter of claims 1-28, nor has a *prima facie* case of obviousness been established. Accordingly, Applicants' claims are patentable over the applied references, as well as general assertions of the claimed features over teachings well known in the art. Withdrawal of the §103 rejection is respectfully requested.

For at least these reasons, Applicants respectfully assert that the independent claims are now patentable over the applied references. The dependent claims are likewise patentable over the applied references for at least the reasons discussed as well as for the additional features they recite. Consequently, all the claims are in condition for allowance. Thus, Applicants respectfully request that the rejections under 35 U.S.C. §§102 and 103 be withdrawn.

V. Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

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JAO:GWT/gwt

Attachment:
Petition for Extension of Time

Date: October 10, 2003

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